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In the Claims:

Claim 1 (currently amended): A method in a processor comprising steps of:

identifying an instruction loop having a plurality of instructions;

fetching said plurality of instructions from a program memory;

storing said plurality of instructions in a register queue comprising a plurality of registers;

determining whether said processor requires execution of said instruction loop;

outputting said plurality of instructions from said register queue when said processor requires execution of said instruction loop;

executing said plurality of instructions, wherein said executing step comprises;

executing at least one instruction stored in a first register of said plurality of registers,

setting an increment access signal to execute at least one instruction stored in a second register of said plurality of registers, wherein said second register is immediately in sequence after said first register.

Claim 2 (original): The method of claim 1 wherein each of said plurality of instructions in said instruction loop is a VLIW packet.

Claim 3 (original): The method of claim 1 wherein storing one of said plurality of

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instructions in said register queue comprises steps of:

adjusting a head pointer to point to a selected register in said register queue;

writing said one of said plurality of instructions into said selected register.

Claim 4 (original): The method of claim 1 wherein said register queue contains a most recently executed plurality of instructions.

Claim 5 (original): The method of claim 1 wherein said step of determining whether said processor requires execution of said instruction loop comprises checking a PC value.

Claim 6 (original): The method of claim 1 wherein outputting one of said plurality of instructions from said register queue comprises steps of:

adjusting an access pointer to point to a selected register in said register queue;

outputting said one of said plurality of instructions from said selected register.

Claim 7 (original): The method of claim 6 wherein said access pointer is held constant.

Claim 8 (original): The method of claim 6 wherein said access pointer is incremented by one.

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Claim 9 (original): The method of claim 6 wherein said access pointer is decremented by a branch interval.

Claim 10 (original): The method of claim 1 wherein said program memory comprises a cache.

Claim 11 (original): The method of claim 1 wherein said program memory comprises an external memory.

Claim 12 (original): A circuit in a processor comprising:

an instruction fetch module configured to fetch a plurality of instructions, said plurality of instructions belonging to an instruction loop in a program memory;

a register queue configured to store said plurality of instructions, said register queue comprising a plurality of registers;

a tracking module configured to keep track of a desired instruction in said instruction loop;

circuitry for setting an increment access signal to execute at least one instruction stored in a second register of said plurality of registers, wherein said second register is immediately in sequence after a first register of said plurality of registers for which at least one instruction stored therein has just been executed;

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an output module configured to output said desired instruction for decoding and execution by said processor.

Claim 13 (original): The circuit of claim 12 wherein each of said plurality of instructions belonging to said instruction loop is a VLIW packet.

Claim 14 (original): The circuit of claim 12 wherein said tracking module comprises a head pointer configured to point to a selected register in said register queue, wherein said selected register stores said desired instruction.

Claim 15 (original): The circuit of claim 12 wherein said register queue is configured to contain a most recently executed plurality of instructions.

Claim 16 (original): The circuit of claim 12 wherein said instruction fetch module checks a PC value to determine whether said processor requires fetching and execution of said instruction loop.

Claim 17 (original): The circuit of claim 12 wherein said output module comprises an access pointer, said access pointer being configured to point to a selected register in said register queue, wherein said selected register outputs said desired instruction.

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Claim 18 (original): The circuit of claim 17 wherein said access pointer is held constant.

Claim 19 (original): The circuit of claim 17 wherein said access pointer is incremented by one.

Claim 20 (original): The circuit of claim 17 wherein said access pointer is decremented by a branch interval.

Claim 21 (original): The circuit of claim 12 wherein said program memory comprises a cache.

Claim 22 (original): The circuit of claim 12 wherein said program memory comprises an external memory.

Claim 23 (currently amended): A method in a processor comprising steps of:

identifying a loop having a plurality of VLIW packets;

fetching said plurality of VLIW packets from a program memory;

storing said plurality of VLIW packets in a register queue comprising a plurality of registers;

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determining whether said processor requires execution of said loop;

outputting said plurality of VLIW packets from said register queue when said processor requires execution of said loop;

executing said plurality of VLIW packets, wherein said executing step comprises:

executing at least one instruction stored in a first register of said plurality of registers,

setting an increment access signal to execute at least one instruction stored in a second register of said plurality of registers, wherein said second register is immediately in sequence after said first register.

Claim 24 (original): The method of claim 23 wherein storing one of said plurality of VLIW packets in said register queue comprises steps of:

adjusting a head pointer to point to a selected register in said register queue;

writing said one of said plurality of VLIW packets into said selected register.

Claim 25 (original): The method of claim 23 wherein said register queue contains a most recently executed plurality of VLIW packets.

Claim 26 (original): The method of claim 23 wherein said step of determining whether said processor requires execution of said loop comprises checking a PC value.

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Claim 27 (original): The method of claim 23 wherein outputting one of said plurality of VLIW packets from said register queue comprises steps of:

adjusting an access pointer to point to a selected register in said register queue;

outputting said one of said plurality of VLIW packets from said selected register.

Claim 28 (original): The method of claim 27 wherein said access pointer is held constant.

Claim 29 (original): The method of claim 27 wherein said access pointer is incremented by one.

Claim 30 (original): The method of claim 27 wherein said access pointer is decremented by a branch interval.

Claim 31 (original): The method of claim 23 wherein said program memory comprises a cache.

Claim 32 (original): The method of claim 23 wherein said program memory comprises an external memory.

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